PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ferguson, Michael Ian	)	Examiner: KERVEROS, James C
Serial No.:	10/584,592	)	Art Unit: 2117
Filed:	September 11, 2007	)	Our Ref: P752-US
For:	"FINGERPRINTED CIRCUITS AND METHODS OF MAKING AND IDENTIFYING THE SAME"	)	Date: April 11, 2011
		)	Re: ***Amendment and Response***

AMENDMENT AND RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is filed in response to the Office Action mailed on January 14, 2011, a reply to which is initially due April 14, 2011. Please enter the following amendments and remarks.

All amendments and remarks are made without prejudice.

Correction of the title begins on page 2 of this paper

Amendment to the drawings begins on page 3 of this paper.

Amendments to the specification begin on page 4 of this paper.

Amendments to the claims begin on page 6 of this paper.

Remarks begin on page 8 of this paper.

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CORRECTION OF THE TITLE

Please be advised that USPTO records indicate the title of the application incorrectly as "FINGERPRINTED CIRCUITS AND METHODS OF MAKING AND **IDENIFYING** THE SAME". Please be advised that the title as originally filed by the Applicant is "FINGERPRINTED CIRCUITS AND METHODS OF MAKING AND **IDENTIFYING** THE SAME".

Enclosure: Copy of the Transmittal of New Application as originally filed on September 11, 2007.

AMENDMENT TO THE DRAWINGS

Sixteen replacement sheets including FIGS. 1-16 (left unchanged) are being enclosed with the present response. These sixteen sheets replace the original sheets 1-8 including FIGS. 1-16.

Enclosures: Replacement sheets 1/16-16/16, 16 sheets in total.

AMENDMENTS TO THE SPECIFICATION

All amendments are made with reference to the present applicant as originally filed. Paragraph numbers are referenced to the published application No: US 2010/0264204 A1.

1) Please amend the Abstract as follows:

ABSTRACT

A circuit having a fingerprint for identification of a particular instantiation of the circuit is disclosed. The circuit ~~comprises~~ may include a plurality of digital circuits or gates~~, the plurality digital circuits or gates each having an analog input and wherein each of the digital circuits or gates has at least one functional state wherein the corresponding digital circuit or gate performs an intended digital function and at least one other state wherein the intended digital function is not performed~~. Each of the digital circuits or gates is responsive to a configuration voltage applied to its analog input for controlling whether or not the digital circuit or gate performs its intended digital function and each of the digital circuits or gates transitioning between its functional state and its at least one other state when the configuration voltage equals a boundary voltage. The boundary voltage varies between different instantiations of the circuit for a majority of the digital circuits or gates and these differing boundary voltages serving to identify (or fingerprint) different instantiations of the same circuit. ~~A plurality of digital to analog converters are preferably used for generating configuration voltages each applied to one or more of the plurality of digital circuits or gates.~~

2) Please amend paragraph [0001] of the specification, after the section heading "Cross Reference to Related Applications" as follows:

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. patent application Ser. No. 10/526,613 ~~_____~~ and filed April 18, 2005 ~~_____~~ on entitled "Methods of Camouflaging the Functions of Electronic Circuits" and filed, the disclosure of which is hereby incorporated herein by reference.

3) Please amend paragraph [0038] of the specification as follows:

[0038] By the use of an evolutionary algorithm, such as that described in the aforementioned copending U.S. patent application Ser. No. 10/526,613 ~~_____~~, very tightly constrained design topologies can be found that provide consistent circuit/gate functionality in the middle of the configured range *(Ac_{min}* to *Ac_{max})* but have ill-defined configuration range boundaries *(Ac_{min} and Ac_{max})* when fabricated, the resulting circuits have both gross functionality that can be designated a priori to circuit fabrication and have fine detail that can be measured and are unique to each fabricated IC.